DRIVING CIRCUIT FOR FLAT PANEL DISPLAYS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a driving circuit, and in particular, a driving circuit disposed on a flat panel display panel.

2. Description of Related Art

Flat panel displays have been widely applied to the display of monitors or electronic products, due to the development of the photoelectric industry. The state of the art in the field of the flat panel displays has a driving circuit, thin-film transistors and necessary circuits disposed on a glass substrate. Fig. 1 shows a schematic diagram of the conventional circuit for sampling/sustaining video signals of a display pixel. The circuit for sampling/sustaining video signals is disposed on a substrate, and analogous switches 111, 112, 113 are disposed between signal lines 121, 122, 123 and active area (display area) 131. The control gate of the analogous switches 111, 112,113 is respectively connected to the input and output terminals of an inverter circuit 141. The inverter circuit 141 is an output buffer for a sampling signal generator. The input terminal of the inverter circuit 141 is connected to a sampling signal generator (not shown). Hence, a pair of complementary sampling signals are outputted to control the operation of the analogous switches 111, 112, 113 respectively. The analogous switches 111, 112, 113 are connected to the video signal lines 121, 122, 123 respectively to receive analogous video signals.

When the analogous switches 111, 112 113 are physically connected to the inverter circuit 141, and the video signal lines 121, 122, 123, crossover points 151 and 152 in figure 1, for example, between lines by intersection other than connection occur on the signal lines 121 and 123, respectively. It is realized that more crossover points than the points 151 and 152 as shown in the schematic diagram exist in practice. For each video line, a parasitic capacitance occurs on the crossover point, which will result in unwanted power consumption and may cause poor picture quality. Hence, there is a dire need to adequately dispose of the analogous switches 111, 112, 113, the sampling buffer circuit (i.e., the inverter circuit 141) and the signal lines 121, 122, 123 to decrease the quantity of the parasitic capacitances on the video signal lines.

SUMMARY OF THE INVENTION

The primary object of the present invention is to provide a panel for flat panel displays and a driving circuit disposed on the panel to decrease the number of the parasitic capacitances on video lines so as to improve picture quality and to decrease power consumption.

To attain the above-mentioned object, a driving circuit for flat panel displays disposed on a flat panel display panel according to the present invention comprises a plurality of signal lines for providing analogous video signals, at least one buffer unit for inverting a scanning signal, and a plurality of switch units disposed between the signal lines. Each of the switch units is connected to one of the signal lines to receive an analogous video signal, and also, is connected to the output terminal of the buffer unit.

A scanning signal enables the operation of the plurality of switch units so that a video signal is outputted to the active area (display area) of the flat panel display panel.

The disposition between the plurality of switch units of the driving circuit and the active area (display area) of the flat panel display panel according to the present invention is not specifically defined. Preferably, the plurality of switch units and the active area (display area) of the flat panel display panel are spaced apart with at least one signal line. The disposition of the signal lines of the driving circuit according to the present invention is not specifically defined. Preferably, at least one signal line is disposed between the switch units and the buffer unit for inverting a scanning signal. The disposition between the signal lines and the switch units of the driving circuit according to the present invention is not specifically defined. Preferably, the signal lines are disposed between the switch units and the active area (display area). The buffer unit for inverting a scanning signal of the driving circuit according to the present invention is not specifically defined. Preferably, the buffer unit for inverting a scanning signal is an amplification circuit, and more preferably, an inverting amplification circuit, to receive a timing signal, and then, amplify the timing signal to output at least one scanning signal. The flat panel display panel adapted to the driving circuit according to the present invention is not specifically defined. Preferably, the flat panel display panel is an organic light-emitting diode (OLED) display, or a liquid crystal display (LCD). Specifically, the LCD is the most preferred.

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of the conventional circuit for sampling/sustaining signals;

Fig. 2a is a schematic diagram of a driving circuit according to the first embodiment of the present invention;

Fig. 2b is a schematic diagram of the parasitic capacitances associated with the first embodiment of the present invention;

Fig. 3a is a schematic diagram of the driving circuit according to the second embodiment of the present invention;

Fig. 3b is a schematic diagram of the parasitic capacitances associated with the second embodiment of the present invention; and

Fig. 4 is a comparison table of the quantity of the parasitic capacitances according to whether the conventional driving circuit or the driving circuit according to the present invention is used.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference to Fig. 2a, a schematic diagram of a driving circuit for sample/sustenance according to the first embodiment of the present invention is shown. The circuit comprises a plurality of signal lines 211, 212, 213, a plurality of switch units 221, 222, 223, a buffer unit for inverting a scanning signal 231 and an active area (display area) 241. The plurality of signal lines 211, 212, 213 supply analogous video signals; for example, the

signal line 211 supplies an analogous video signal for blue, the signal line 212 supplies an analogous video signal for red, and the signal line 213 supplies an analogous video signal for green.

In this embodiment, the buffer unit for inverting a scanning signal 231 is preferably an inverter circuit. The input terminal of the inverter circuit is connected to a scanning signal generator (not shown). The scanning signal generator supplies a positive phase timing signal to drive an N-type metal-oxide-silicon field-effect-transistor (NMOSFET) of the plurality of switch units 221, 222, 223. The buffer unit for inverting a scanning signal 231 receives the positive phase timing signal outputted from the scanning signal generator, and then, supplies an inverted signal (that is, a negative phase timing signal) to drive a P-type metal-oxide-silicon field-effect-transistor (PMOSFET) of the plurality of switch units 221, 222, 223.

In this embodiment, the plurality of switch units 221, 222, 223 can be of any electronic switches, and preferably, transistors, and more preferably, thin film transistors (TFTs). The plurality of switch units 221, 222, 223 are disposed between the signal line 212 and the signal line 213. Each n-type control gate of the switch units 221, 222, 223 is connected to the input terminal of the buffer unit and each p-type control gate of the switch units 221, 222, 223 is connected to the output terminal of the buffer unit 231. The switch units 221, 222, 223 are connected to the signal lines 211, 212, 213 respectively. The scanning signals control the output of the plurality of switch units 221, 222, 223. With the arrival of the scanning

signals, the plurality of switch units 221, 222, 223 output the video signals to data lines (not shown) in the active area (display area) 241 through output signal lines 2211, 2221, 2231.

Fig. 2b shows a schematic diagram of the parasitic capacitances associated with the first embodiment of the present invention. The parasitic capacitance per pixel length on the video line 211 comes from crossover points 411, 412, 413 (as denoted in the three triangles in Fig. 2b) where the signal line wire intersects the signal line 212 and lines 2311, 2312 connecting the buffer unit 231 and the plurality of switch units 221, 222, 223. The parasitic capacitance per pixel length on the video lines 212 comes from crossover points 421, 422, 423 (as denoted in the three squares in Fig. 2b) where the signal line wire intersects the buffer unit 231 and the lines 2311, 2312 connecting the plurality of switch units 221, 222, 223. The parasitic capacitance per pixel length on the video line 213 comes from crossover points 431, 432, 433 (as denoted in the three hexagons in Fig. 2b) where the signal line wire intersects the output signal lines 2211, 2221, 2231 of the plurality of switch units 221, 222, 223. Therefore, within a pixel length each video line has a parasitic capacitance from three crossover points for this embodiment. Figure 3a shows a schematic diagram of the driving circuit for sample/sustenance according to the second embodiment of the present invention. The components and the line connections of the second embodiment are similar to those of the first embodiment, except a plurality of switch units 321, 322, 323 disposed between a signal line 313 (for providing an analogous video signal for green) and a signal line 311

(for providing an analogous video signal for blue) as well as two signal lines 311, 312 used to space the plurality of switch units 321, 322, 323 from an active area (display area) 341.

Fig. 3b shows a schematic diagram of the parasitic capacitances associated with the second embodiment of the present invention. The parasitic capacitance per pixel length on the video line 311 is due to crossover points 451, 452, 453, 454 (as denoted in four triangles in Fig. 3b) where the signal line wire intersects output signal lines 3211, 3221, 3231 of the plurality of switch units 321, 322, 323 and a line 3222 connecting the switch unit 322 to the signal line 312. The parasitic capacitance per pixel length on the video line 312 is due to crossover points 461, 462, 463, 464 (as denoted in four hexagons in Fig. 3b) where the signal line wire intersects the output signal lines 3211, 3221, 3231 of the plurality of switch units 321, 322, 323 and the signal line 311. The parasitic capacitance per pixel length on the video line 313 is due to crossover points 441, 442 (as denoted in two squares in Fig. 3b) where the signal line wire intersects lines 3311, 3312 connecting the buffer unit 331 and the plurality of switch units 321, 322, 323.

Fig. 4 is a comparison table of the number of the crossover points per pixel length on the video lines according to whether the conventional driving circuit or the driving circuit according to the present invention is used. As shown in this table, 12 crossover points (i.e., 4 crossover points for each video line) within one pixel length are associated with the conventional driving circuit while only nine crossover points (i.e., 3

crossover points for each video line) within one pixel length are associated with the layout according to the first embodiment of the present invention and 10 parasitic capacitances within one pixel length are associated with the layout according to the second embodiment of the present invention. Therefore, the circuit of the present invention can decrease the amount of the parasitic capacitance on video lines, improve picture quality at high video sampling rate, and decrease dynamic power dissipation on video lines.

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.